WHAT IS CLAIMED IS:

1. A method for accessing an array of memory cells arranged as a plurality of rows and columns, comprising:

receiving an address corresponding to a defective row having a defective memory cell;

disconnecting the defective row from true and complementary bit line pairs, each of which is coupled to a respective column of the plurality of columns and periodically interchanged in location at a boundary between groups of the plurality of rows;

connecting a row neighboring the defective row and all rows succeeding the neighboring row to the true and complementary bit line pairs;

connecting a redundant row neighboring the array of memory cells to the true and complementary bit line pairs; and

inverting data at the boundary between groups of the plurality of rows.

2. The method as recited in claim 1, wherein said connecting a row comprises replacing the defective row and all succeeding rows within the array with the neighboring row and all rows succeeding in address value the neighboring row address value.

3. The method as recited in claim 1, wherein said succeeding comprises all address values below an address value of the neighboring row.

4. The method as recited in claim 1, wherein said succeeding comprises all address values above an address value of the neighboring row.

5. The method as recited in claim 1, wherein said inverting comprises inverting the logic value of the data within a row neighboring the boundary.

6. The method as recited in claim 1, wherein said connecting a row and connecting a redundant row comprises shifting the address value of the defective row and all successive rows to the next address value, either upward or downward, to include a redundant row address for each defective row.

7. A semiconductor memory, comprising:

an array of memory cells arranged as a plurality of rows and columns;

a plurality of true and complementary bit line pairs, each of which is coupled to a respective column of the plurality of columns and periodically interchanged in location at a boundary between groups of the plurality of rows; and

circuitry for replacing a row among the plurality of rows having a defective memory cell with another row among the plurality of rows having the next lower address value and inverting the data at the boundary between the groups.

8. The semiconductor memory as recited in claim 7, further comprising a built-in-self-test (BIST) circuit that detects the row having the defective memory cell and stores an address of said row within a latch.

9. The semiconductor memory as recited in claim 7, wherein the circuitry comprises an address decrementing circuit that (i) substitutes the next lower address value for the address of the row having the defective memory cell, and (ii) substitutes the next lower address value for each of the addresses lower than the row having the defective memory cell.

10. The semiconductor memory as recited in claim 7, wherein the boundary separates a pair of rows within the plurality of rows, and wherein one of the pair of rows has an address at the next higher address value than the other of the pair of rows.

11. The semiconductor memory as recited in claim 10, wherein the circuitry comprises:

an address decrementing circuit that decrements an address of said one of the pair of rows to an address of said another of the pair of rows; and

a data inverting circuit that receives data from each row among the plurality of rows and inverts the data within said one of the pair of rows.

12. The semiconductor memory as recited in claim 7, further comprising a plurality of redundant rows of memory cells.

13. The semiconductor memory as recited in claim 12, wherein the circuitry comprises a replacement circuit that replaces a lowest addressable row among the plurality of rows with a highest addressable row among the plurality of redundant rows.

14. A semiconductor memory, comprising:

an array of memory cells arranged as a plurality of rows and columns;

a plurality of true and complementary bit line pairs, each of which is coupled to a respective column of the plurality of columns and periodically interchanged in location at a boundary between groups of the plurality of rows; and

circuitry for replacing a row among the plurality of rows having a defective memory cell with another row among the plurality of rows having the next higher address value and inverting the data at the boundary between the groups.

15. The semiconductor memory as recited in claim 14, further comprising a built-in-self-test (BIST) circuit that detects the row having the defective memory cell and stores an address of said row within a latch.

16. The semiconductor memory as recited in claim 14, wherein the circuitry comprises an address incrementing circuit that (i) substitutes the next higher address value for the address of the row having the defective memory cell, and (ii) substitutes the next higher address value for each of the addresses higher than the row having the defective memory cell.

17. The semiconductor memory as recited in claim 14, wherein the boundary separates a pair of rows within the plurality of rows, and wherein one of the pair of rows has an address at the next lower address value than the other of the pair of rows.

18. The semiconductor memory as recited in claim 17, wherein the circuitry comprises:

an address increasing circuit that increases an address of said one of the pair of rows to an address of said another of the pair of rows; and

a data inverting circuit that receives data from each row among the plurality of rows and inverts the data within said one of the pair of rows.

19. The semiconductor memory as recited in claim 14, further comprising a plurality of redundant rows of memory cells.

20. The semiconductor memory as recited in claim 19, wherein the circuitry comprises a replacement circuit that replaces a highest addressable row among the plurality of rows with a lowest addressable row among the plurality of redundant rows.